



PRODUCT SPECIFICATION

KADI Model: KD123EWUNN-FL

CUSTOMER Model:

Description: 12.3" OLED Module with LENS

Version: 1.0

KADI	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2024.12.5	2024.12.5	2024.12.5

CUSTOMER APPROVAL	SIGNATURE	DATE



Record of Revisions

Version	Revise Date	Description	Page
1.0	2024-12-5	First Release	-



Contents

1. General Specifications	4
2. Electrical Characteristics	5
3. I/O Connection and Block Diagrams	7
4. Timing Characteristics	10
5. Reset Timing Sequence Requirement	12
6. Optical Specifications	16
7. Reliability Test Items	20
8. Mechanical Drawing	21
9. Packing	22
10. Precautions for Use of OLED modules	23



1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
OLED Size	12.3	inch
Number of Pixels	3000 (H) RGB x 1920 (V)	pixels
Viewing Direction	Free	o' clock
Interface	MIPI 8 lanes	-
Display Colors	10 bits	colors
Outline Dimension	272.86(W)*178.58 (H) *1.686 (T)	mm
Active Area	263.16 (H) x 168.42 (V)	mm
Pixel Pitch	87.72 (H) x87.72 (V)	um
Driver IC	HX83211	-
Operation Temperature	-20~70	°C
Storage Temperature	-30~80	°C
Display frequency	60/120/144Hz Switchable	

Note1:

Requirements on Environmental Protection: RoHS Compliant



2. Electrical Characteristics

2.1 DC Characteristics Requirements

Item	Symbol	Min.	Typ.	Max.	Unit	Note
TP Power supply	Touch_AVDD	2.7	3.3	3.4	V	Despond on the TSP IC
DDIC Power supply	VCI	2.7	3.3	3.6	V	
DDIC I/O Supply Voltage	VDDI	1.65	1.8	1.98	V	
DDIC Charge pumping Power	AVDD	7.15	7.3	7.45	V	
EL supply voltage	ELVDD	4.5	4.6	4.7	V	DC/DC output
EL supply voltage	ELVSS	-4.3	-4.2	-4.1	V	HBM Controlled by DDIC
EL supply voltage	ELVSS	-3.8	-3.7	-3.6	V	Normal luminance Controlled by DDIC
EL supply voltage	ELVSS	-4.3	-3~3.8	-2.9	V	
EL supply voltage	ELVSS	-3.2	-3	-2.9	V	150nit~minimum luminance Controlled by DDIC
Input High Voltage	VIH	-	-	460	mV	MIPI HS
Input Low Voltage	VIL	-40	-	-	mV	MIPI HS
Input High Voltage	VIH	880	-	-	mV	MIPI LP
Input Low Voltage	VIL	-	-	550	mV	MIPI LP
Input High Voltage	VIH	1100	1200	1300	mV	MIPI LP
Input Low Voltage	VIL	-50	-	50	mV	MIPI LP
Frame Frequency	fFRAME	59	60	61	Hz	Command mode
		142	144	146	Hz	Command mode

Note 1:

DDIC OSC frequency : 102Mhz \pm 1%



2.2 Power Consumption of Display Panel and Touch panel

2.2.1 For Display panel

For Display panel with normal brightness ~400nit.

Condition: ACL off, still pattern, Normal mode (not Seed mode)

Power Supply: VDDI=1.8V 、 VCI=3.3V 、 AVDD=7.3V 、 ELVDD=4.6V 、 ELVSS=-3.7V

- Normal mode (Power consumption is not satisfied in Seed and HBM mode)

Frame Frequency: fFRAME=60Hz @ 25degC

Display Mode	Item	Typ.	Max.	Unit	Note
Display White	Total	8245	9070	mW	600nit,60HZ

- Deep Standby Mode: IC Power on+ reset high
- Sleep in: With CMD 28 10 + reset keep high

2.2.2 For TP (Fix a full black pattern and then test):

Power Supply: TP AVDD=3.3V

Report Rate: Display panel Frame Frequency = 60Hz



3. I/O Connection and Block Diagrams

3.1 Main I/O Connection

CN1

No.	Symbol	Description
1	GND	Ground
2	NC	No connection
3-6	VDD	Power supply
7	NC	No connection
8-17	ELVDD	Positive power supply for EL
18	NC	No connection
19-28	ELVSS	Negative power supply for EL
29	NC	No connection
30-33	GND	Ground
34	NC	No connection
35	TP_Report_EN	Open, for test use only
36	TP_GPIO	
37	TP_RST	Reset the TSP IC
38	TP_INT	TSP INT from AP
39	TP_SPI_CS0	Touch chip select for SPI I/F
40	TP_SPI_SCK	Touch CLK for SPI I/F
41	TP_SPI_MOSI	Touch MOSI for SPI I/F
42	TP_SPI_MISO	Touch MISO for SPI I/F
43	TP_SDA	Pad for TSP SDA
44	TP_SCL	Pad for TSP SCL
45	NC	No connect
46	TP_3.3V	Analog Power for TSP
47	NC	No connect
48	GND	Ground
49	I2C_M_SCL	
50	I2C_M_SDA	
51	GND	Ground



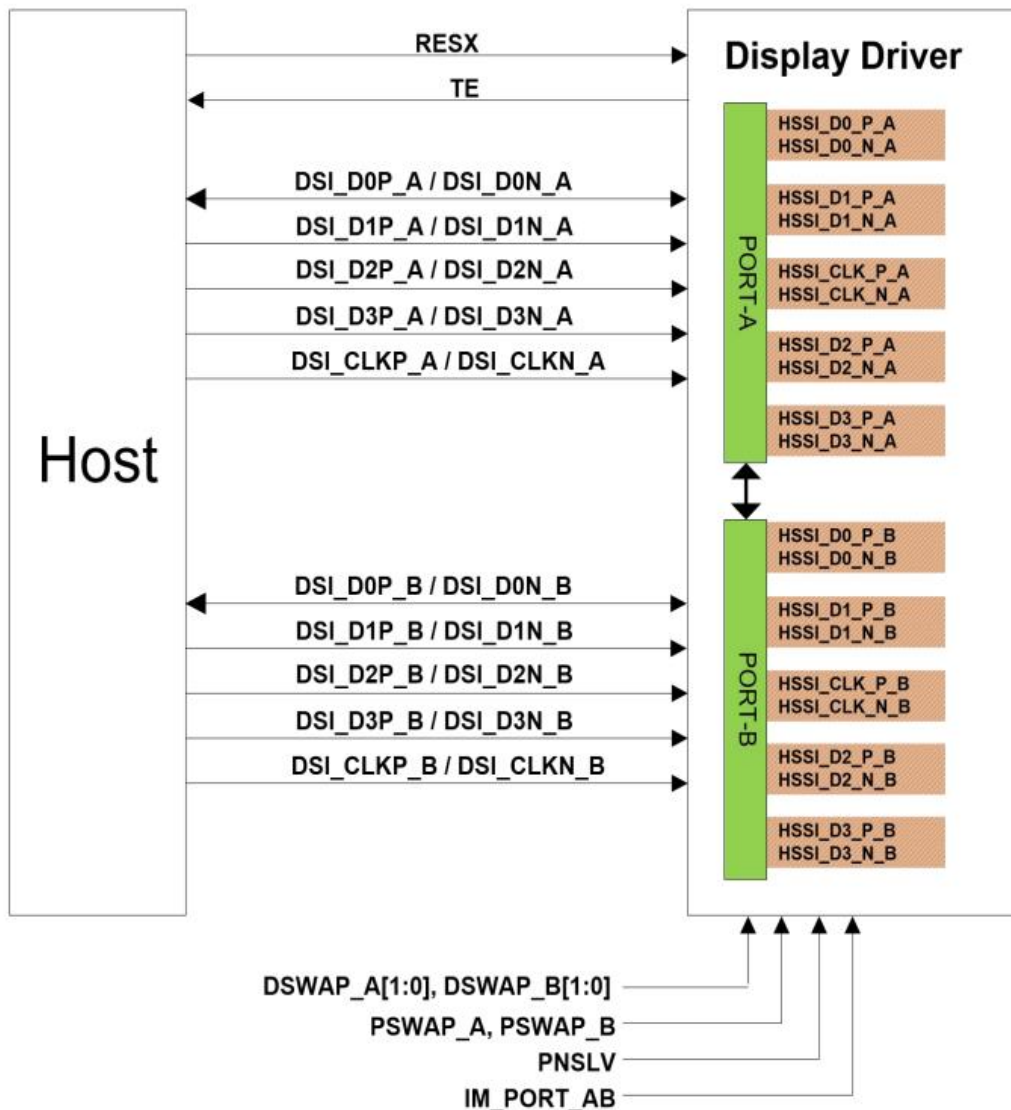
CN2

No.	Symbol	Description
1	NC	No connection
2	TCON_RDY	TCON Ready
3	TCON_RST	TCON Reset
4	TCON_TE	Tearing effect signal
5	TCON_ESD	
6	NC	No connect
7	NC	No connect
8	OLED_ID1	ID
9	NC	No connect
10	AVDD	Power Supply 7.15-7.45V(7.3V)
11	NC	No connect
12	OLED_EN	
13	SWIRE	
14	BIST_EN	BIST enable signal
15	GND	Ground
16-19	NC	No connect
20	GND	Ground
21	RX0_D3_N	DSI-D3-of IC MIPI
22	RX0_D3_P	DSI-D3-of IC MIPI
23	GND	Ground
24	RX0_D2_N	DSL-D2- of IC MIPI
25	RX0_D2_P	DSL-D2- of IC MIPI
26	GND	Ground
27	RX0_C0_N	MIPI DSI CLOCK-
28	RX0_C0_P	MIPI DSI CLOCK+
29	GND	Ground
30	RX0_D1_N	DSL-D1- of IC MIPI
31	RX0_D1_P	DSL-D1- of IC MIPI
32	GND	Ground
33	RX0_D0_N	DSI-D0- of IC MIPI
34	RX0_D0_P	DSI-D0- of IC MIPI
35	GND	Ground
36	GND	Ground
37	RX1_D3_N	DSI-D3- of IC MIPI
38	RX1_D3_P	DSI-D3- of IC MIPI
39	GND	Ground
40	RX1_D2_N	DSI-D2- of IC MIPI
41	RX1_D2_P	DSI-D2- of IC MIPI



42	GND	Ground
43	RX1_C0_N	MIPI DSI CLOCK-
44	RX1_C0_P	MIPI DSI CLOCK+
45	GND	Ground
46	RX1_D1_N	DSI-D1- of IC MIPI
47	RX1_D1_P	DSI-D1- of IC MIPI
48	GND	Ground
49	RX1_D0_N	DSI-D0- of IC MIPI
50	RX1_D0_P	DSI-D0- of IC MIPI
51	GND	Ground

3.2 MIPI-DSI Reference Circuit

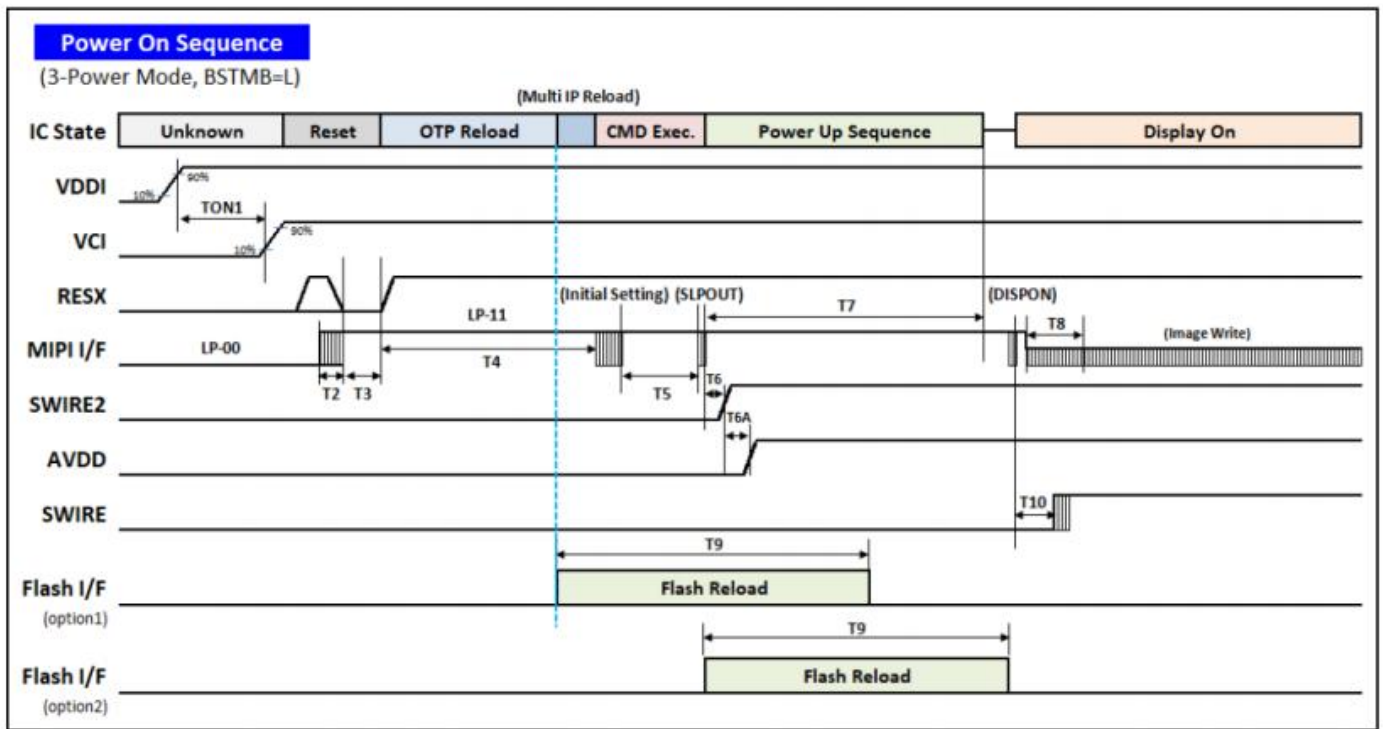




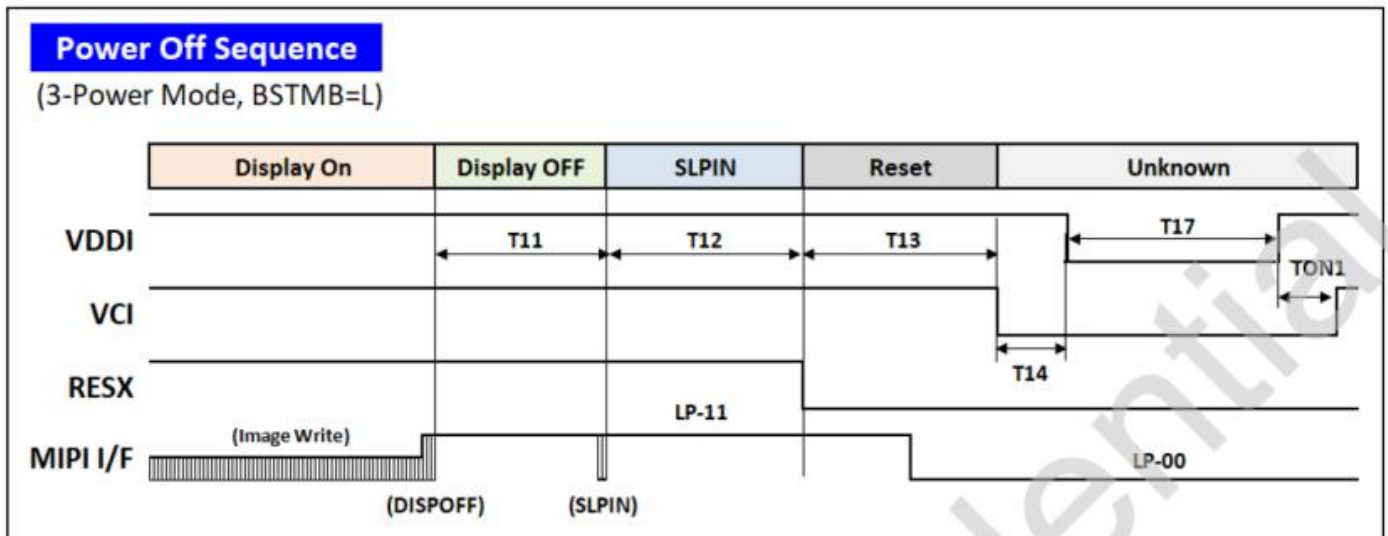
4. Timing Characteristics

4.1 Power on/off Sequence

4.1.1 Power on sequence



4.1.2 Power off sequence





Timing Specification of Power On/Off Sequence

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
TON1	2	-	-	ms	VDDI-to-VDDI Power Ready Timing (for 3-Power Mode)
TON2	0	-	-	ms	VDDI-to-DVDD Power Ready Timing (for 4-Power Mode)
TON3	2	-	-	ms	DVDD-to-VCI Power Ready Timing (for 4-Power Mode)
T2	1	-	-	ms	MIPI stabilization time
T3	1	-	-	ms	Effective hardware reset period
T4	32	-	-	ms	Initial code input starts to RESX goes H. T4 contains OTP Reload + Multi IP Reload inside Flash IC, Note (1)
T5	0	-	-	ms	Initial code input finish to SLPOUT command input
T6	0	-	16	ms	SWIRF2 goes H after SI POUT cmd, Note (2)
T6A	0	-	16	ms	AVDD starts after SWIRE2 goes H
T7	6	6	6	VS	Normal power-up sequence, Note (3)
T8	2	-	14	VS	Display-On Blanking region, Note (4)
T9	0	80	-	ms	16Mb Quad-SPI Flash reload time, Note (5)
T10	1	-	7	VS	SWIRE enable after receiving DISPON cmd, Note (6)
T11	1	-	14	VS	Display Off Blanking region
T12	1	-	-	VS	Power Off Blanking region
T13	2	-	-	ms	Effective hardware reset period
T14	2	-	-	ms	Power off period (for 3-Power Mode)
T15	2	-	-	ms	Power off period (for 4-Power Mode)
T16	0	-	-	ms	Power off period (for 4-Power Mode)
T17	5	-	-	ms	Power down period, Not (7)

Note 1:

The timing is reserved for safe operation of initial setting from OTP reload + Multi IP reload (inside Flash) after RESET event. The OTP reload time depends on the total Page Numbers of OTP that are written in the DDIC. The Multi IP reload time depends on the Multi IP setting numbers inside the Flash IC.

Note 2:

It depends on external power IC spec, and it is suggested to use SWIRE2 to control external Power IC directly.

Note 3:

The power-up sequence is equal to 6VS. The VS timing can be different from DISPON VS. That means normally power-up VS is 60Hz, if user needs to reduce power on timing, the power-up VS can be boosted to 120Hz while keeps DISPON VS at 60Hz.

Note 4:

The SWIRE signal is to control OVDD/OVSS generated from external Power IC. The OVDD/OVSS must be enabled within 15ms after SWIRE goes H.

Note 5:

The typical $T9 = \text{Flash Size} / 50\text{MHz} / \text{Wire Number} = 16\text{Mb} / 50\text{MHz} / 4 = 80\text{ms}$.



Note 6:

VS means the time period of a complete display frame which is approximately 16ms if internal display timing is used.

Note 7:

The power down period defines the minimum OFF time when the power is down for a while.

Note 8:

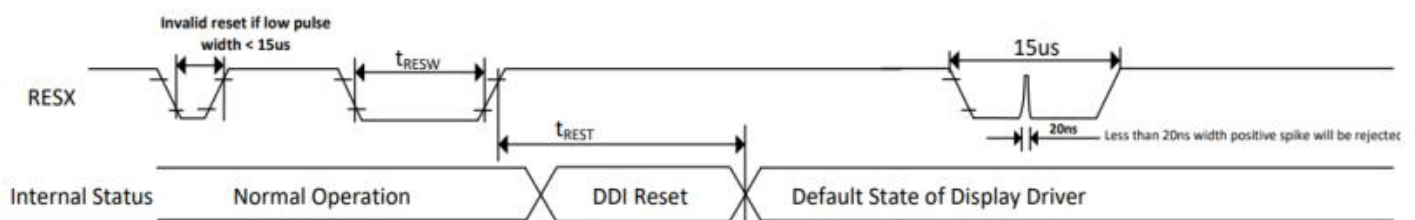
For all items. Those remarked "." (don't care symbol) means no limitation for the timing.

5. Reset Timing Sequence Requirement

5.1 Display panel reset timing:

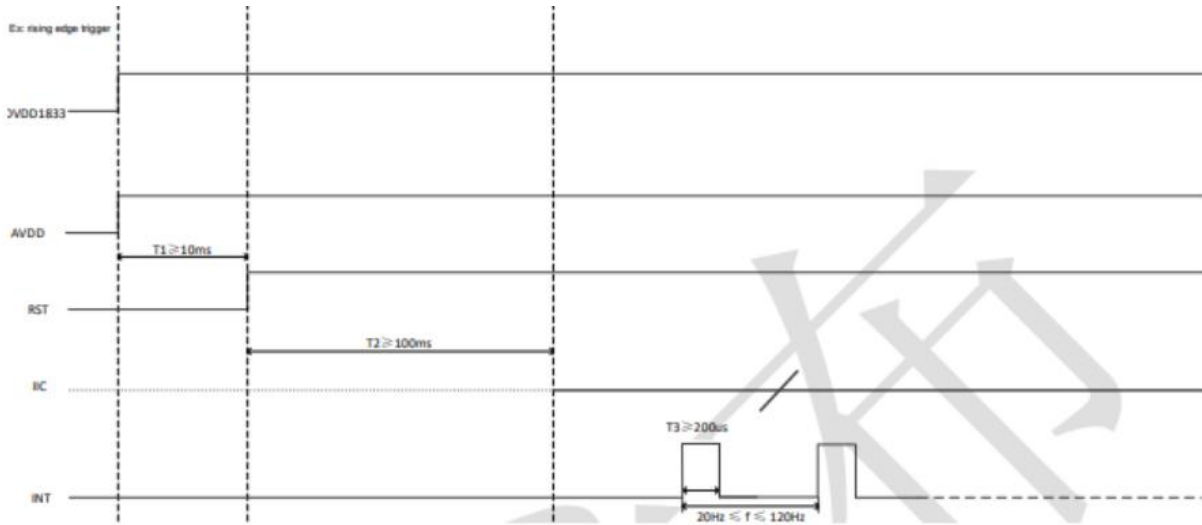
Item	Symbol	Unit	Min	Typ	Max
Reset low-level width	t_{RESW}	us	15		
Reset complete time (during sleep in mode)	t_{REST}	ms			10
Reset complete time (during sleep out mode)	t_{REST}				120

t_{RESW} shorter than 5us, Reset will be rejected.



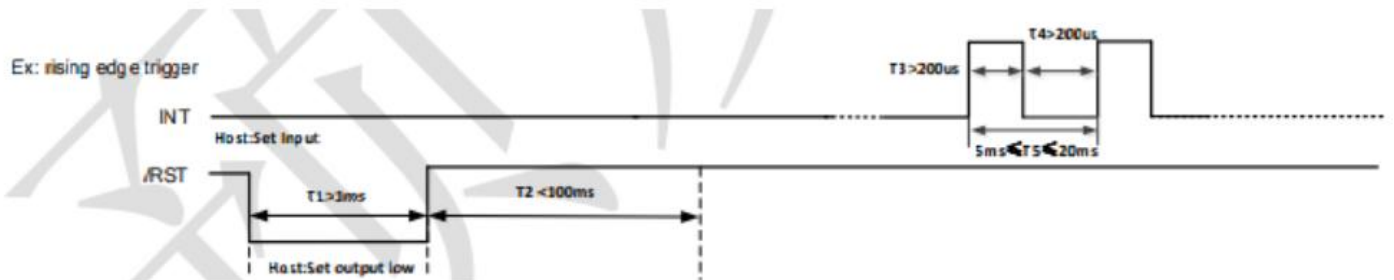


5.2 TP reset timing:



Item	min	max
T1	2 ms	
T2	100 ms	
T3	200 us	

TP Reset timing:



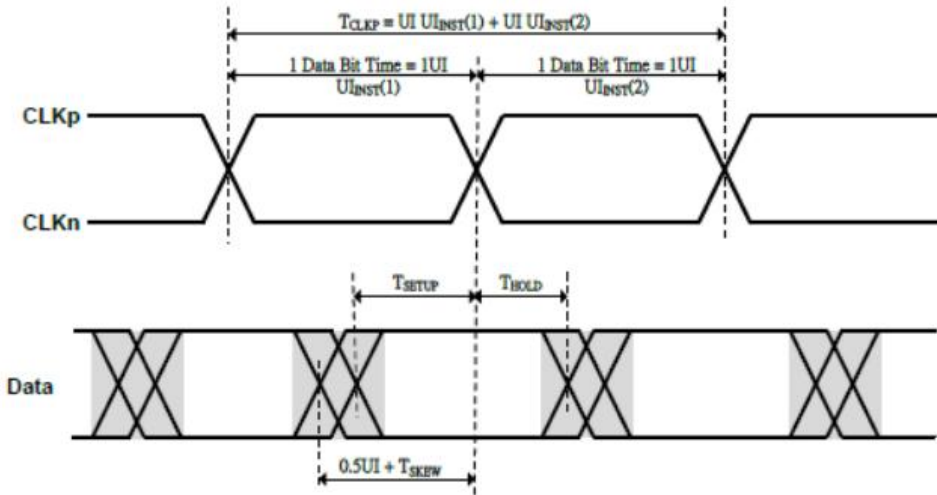


5.3 MIPI 8 lanes Interface Characteristics

5.3.1 High speed mode

High Speed Data Transmission: Data-Clock Timing

■ Data to Clock Timing Definitions



■ Data-Clock Timing Specifications:

Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	1		12.5	ns	1,2
Data-to-Clock Skew	T_{SKEW}	-0.15		0.15	UI_{INST}	3
Data-to-Clock Setup Time (Receiver side)	T_{SETUP}	0.15			UI_{INST}	4
Clock-to-Data Hold Time (Receiver side)]	T_{HOLD}	0.15			UI_{INST}	4

Note 1:

This value corresponds to a minimum 80 Mbps data rate.

Note 2:

The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Note 3:

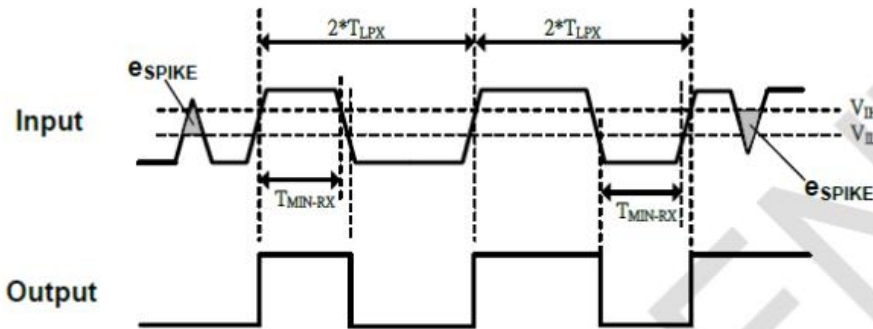
Total silicon and package delay budget of $0.3 \cdot UI_{INST}$

Note 4:

Total setup anoreceier of $0.3 \cdot UI_{INST}$



5.3.2 Low power mode



Low-Power Receiver Specifications

Parameter	Description	Min	Nom	Max	Units	Note
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input hysteresis	25			mV	
eSPIKE	Input pulse rejection			300	V*ps	1
TMIN-RX	Minimum pulse width response	20			ns	

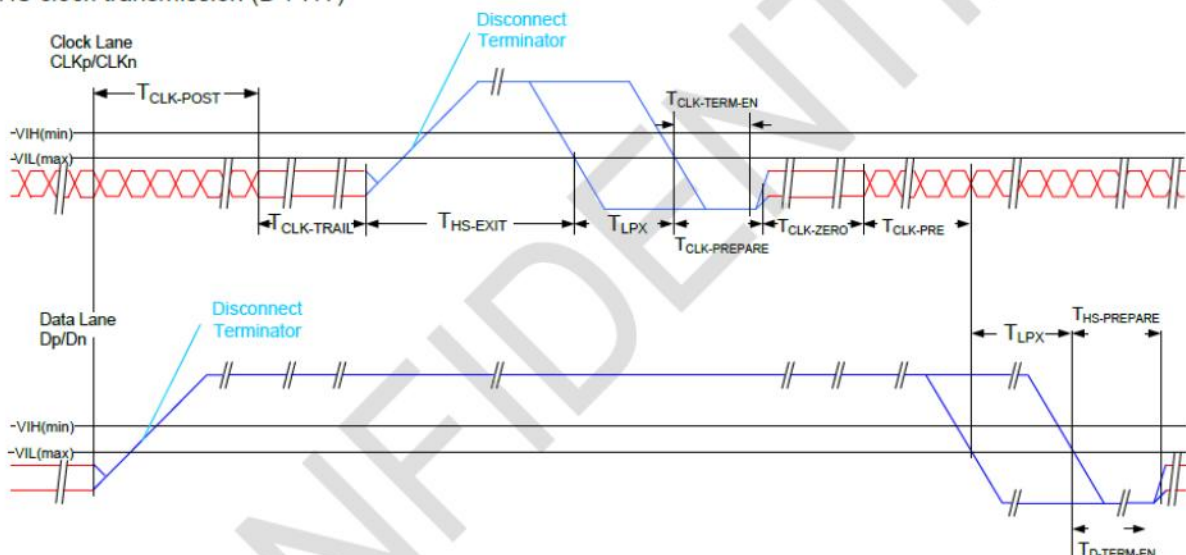
Note 1:

Time-voltage integration of a spike above V_{il} when being in LP-0 state or below V_m when being in LP-1 state. An impulse less than this will not change the receiver state. An input pulse greater than this shall toggle the output.

5.3.3 Switching Clock lane

Switching the Clock Lane between Clock Transmission and Low-Power Mode

HS clock transmission (D-PHY)





6. Optical Specifications

Test condition:

Condition: ACL off, still pattern, Normal mode

Power Supply: VDDI=1.8V VCI=3.3V AVDD=7.3V ELVDD=4.6V, with dynamic ELVSS: ELVSS= -4.3V~3.1V@600nit~4nit

Frame Frequency: fFrame = 60Hz&144Hz @25degC

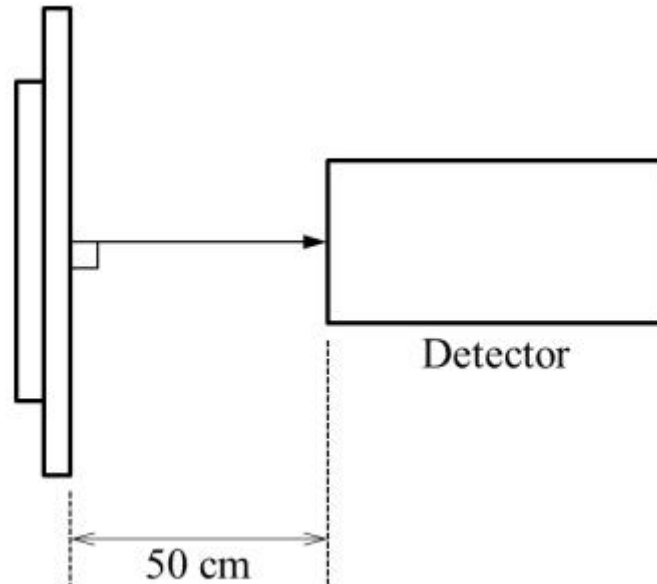
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	$\Phi=90^\circ$ (12 o'clock)	75	80	-	deg	Note2
	θ_B	$\Phi=270^\circ$ (6 o'clock)	75	80	-	deg	Note2
	θ_L	$\Phi=180^\circ$ (9 o'clock)	75	80	-	deg	Note2
	θ_R	$\Phi=0^\circ$ (3 o'clock)	75	80	-	deg	Note2
Response Time	T	ormal $\theta=\Phi=0^\circ$	-	-	2	msec	Note4
Contrast Ratio	CR		100000	-	-	-	Note1 Note3
Color Chromaticity	W_x		0.289	0.299	0.309	-	Note1 Note5
	W_y		0.305	0.315	0.325	-	Note1 Note5
Brightness	L		540	600	660	cd/m ²	Note1 Note7
High Brightness Mode	L		585	650	715	cd/m ²	Note1 Note7
Luminance Uniformity	Y_U		70	80	-	%	Note1 Note6
NTSC	-		-	108	-	%	-
OLED Life Time	-	At 25°C, with white color pattern lighted on, the brightness reduce to 0.5*typ brightness	15000			hrs	



Note 1: Luminance Measurement

Environmental conditions: Temp. $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$, $65 \pm 20\% \text{RH}$, Dark Room.

The data are measured after OLEDs are lighted on for more than 5 minutes and displays are fully white. The brightness is the average value of 9 measured spots. Measurement equipment: CS2000 or similar equipment. (Field of view: 1 deg., Distance: 50 cm)



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

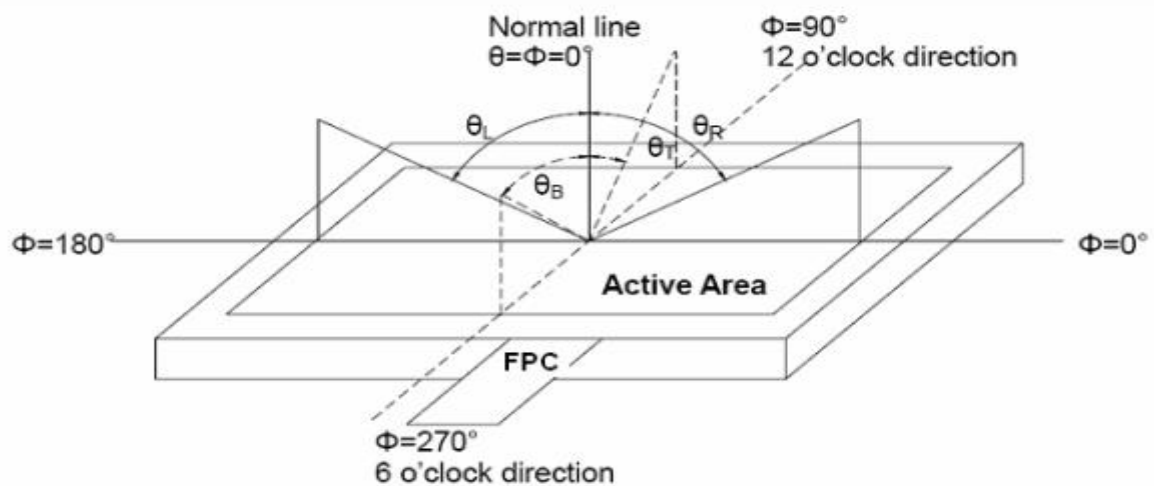


Fig. 1 Definition of viewing angle

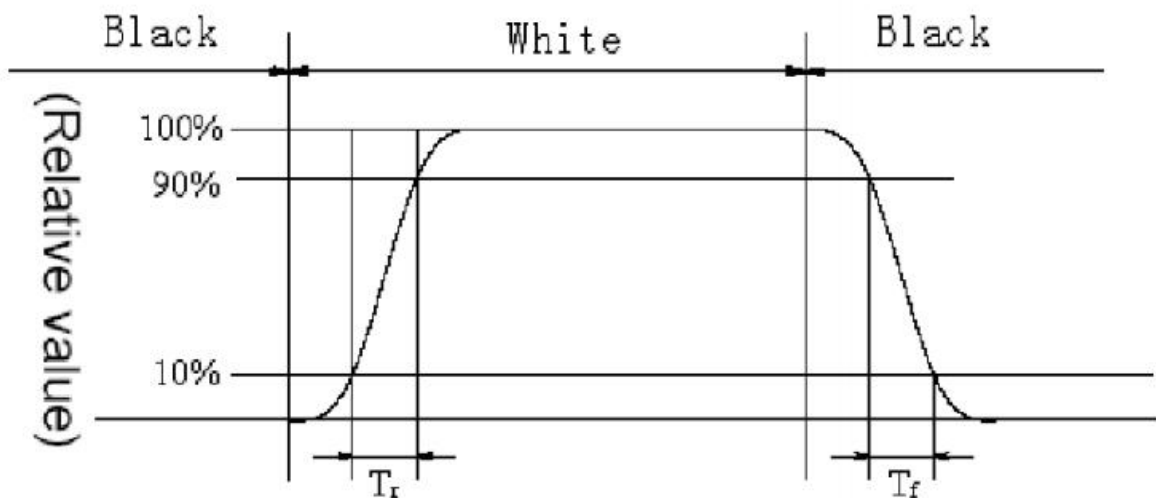


Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (voltage falling time) and from “white” to “black” (voltage rising time), respectively. The response time is defined as the time interval between 10% and 90% of the amplitudes, as shown in the figure below:



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of OLED.

Note 6: Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2

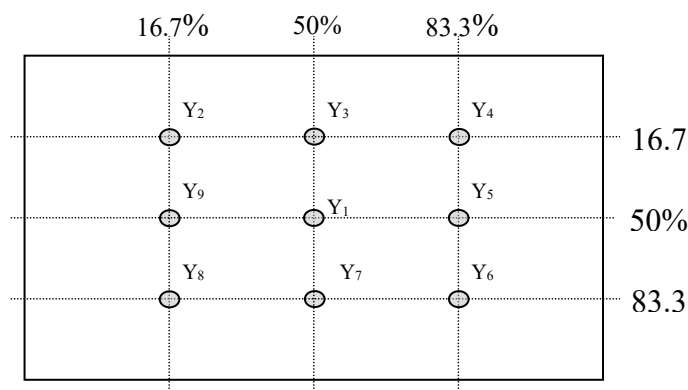


Fig. 2 Definition of points



Note 7: Definition of Luminance (Refer Fig. 2):

Surface luminance is the luminance with all pixels displaying white.

L_v = Average Surface Luminance with all white pixels($P_1, P_2, P_3, \dots, P_n$)



7. Reliability Test Items

Test Item	Test Conditions
High Temperature Storage	Ta= +80°C 96hrs
Low Temperature Storage	Ta= -30°C 96hrs
High Temperature Operation	Ta= +70°C 96hrs
Low Temperature Operation	Ta= -20°C 96hrs
High Temperature and Humidity Operation	Ta= +60°C, 90% RH 96hrs
Thermal Shock (Non-operation)	-30°C/30 min ~ +80°C/30 min for 20 cycles Start with cold temperature, end with high temperature
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction
Package Drop Test	Height: 60 cm, 1 corner, 3 edges, 6 surfaces

Notes:

1. The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

- 1). Air bubble in the OLED
- 2). Seal leak or Glass crack
- 3). Non display or abnormal display
- 4). Brightness reduction >50%



8. Mechanical Drawing

Front view

Side view

Rear view

PN1	SYMBLE	PN1	SYMBLE
1	GND	1	NC
2	NC	2	TCOIN ADY
3	VDD	3	TCOIN ADY
4	VDD	4	TCOIN ADY
5	VDD	5	TCOIN ADY
6	VDD	6	TCOIN ADY
7	NC	7	NC
8	EVDD	8	EVDD
9	EVDD	9	NC
10	EVDD	10	EVDD
11	EVDD	11	NC
12	EVDD	12	EVDD
13	EVDD	13	EVDD
14	EVDD	14	EVDD
15	EVDD	15	EVDD
16	EVDD	16	EVDD
17	EVDD	17	EVDD
18	NC	18	NC
19	EVSS	19	EVSS
20	EVSS	20	EVSS
21	EVSS	21	EVSS
22	EVSS	22	EVSS
23	EVSS	23	EVSS
24	EVSS	24	EVSS
25	EVSS	25	EVSS
26	EVSS	26	EVSS
27	EVSS	27	EVSS
28	EVSS	28	EVSS
29	NC	29	NC
30	GND	30	GND
31	GND	31	GND
32	GND	32	GND
33	GND	33	GND
34	NC	34	NC
35	TP Report EN	35	TP Report EN
36	TP GND	36	TP GND
37	TP RST	37	TP RST
38	TP INT	38	TP INT
39	TP SPI CS0	39	TP SPI CS0
40	TP SCK	40	TP SCK
41	TP SPI MISO	41	TP SPI MISO
42	TP SPI MOSI	42	TP SPI MOSI
43	TP SDA	43	TP SDA
44	TP SCL	44	TP SCL
45	NC	45	NC
46	TP 3.3V	46	TP 3.3V
47	NC	47	NC
48	GND	48	GND
49	IC2 M SCL	49	IC2 M SCL
50	IC2 M SDA	50	IC2 M SDA
51	GND	51	GND

OLET NOTES:

1. DISPLAY TYPE: 12.3 INCH AMOLED
2. OPERATING TEMP: -20°C~+70°C
3. STORAGE TEMP: -30°C~+80°C
4. SOURCE ICRW98110
5. Luminance:600(Typ), 540(Min)
6. (*)reference dimension,**critical dimension
7. Rohs Compliant

REV.	DATE	MODIFICATION	DIRECTION	VIEWING DIRECTION	FREE	PROJECTION	UNIT	SCALE
1.0	2024-11-27	First Issue	Opp	Opp	FREE	3rd ANGLE	mm	1:1

KADI DISPLAY

Material code: TBD

Part No: K0123EWINHFL

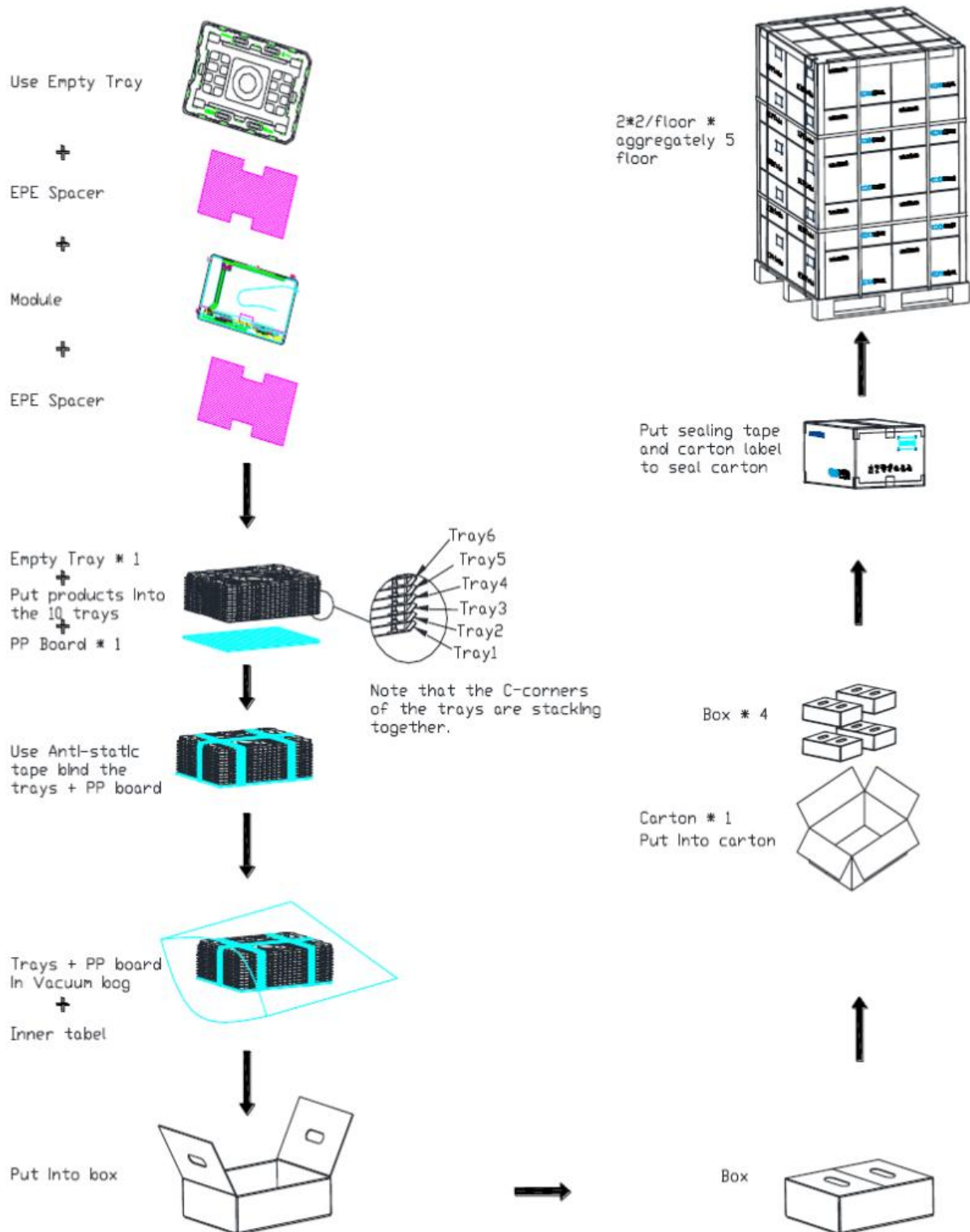
Rev: V1.0 Sheet Of: 1/1

Checked: LHF 2024-11-27 Tolerance: UNLESS SPECIFIED ±0.2



9. Packing

Packing Method





10. Precautions for Use of OLED modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the OLED module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the OLED Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the OLED Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The OLED Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1. When storing the OLED modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2. The OLED modules should be stored under the storage temperature range. If the OLED modules will be stored for a long time, the recommend condition is:

Temperature : 0°C ~ 40°C Relatively humidity: ≤80%

10.2.3. The OLED modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The OLED modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.