PRODUCT SPECIFICATION

KADI Model: KD101QWU88FP-FC85-I04

CUSTOMER Model: -

Description: 10.1 ” TFT-LCD Module with CTP

Version: 1.0

KADI	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2024.6.27	2024.6.27	2024.6.27

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Record of Revisions

Version	Revise Date	Description	Page
1.0	2024-6-14	First Release	-
	2024-6-27	Updated the description of the interface definition and the timing part	7,8

Contents

1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	10.1	inch
Number of Pixels	1200 (H) RGB x 1920 (V)	pixels
Display Mode	Normally Black	-
Viewing Direction	Free	o' clock
Interface	MIPI	-
Display Colors	16.7M	colors
Outline Dimension	244.08 (H) x 162.86 (V) x 7.80 (D)	mm
Active Area	135.36 (H) x 216.58 (V)	mm
Pixel Pitch	0.1128 (H) x 0.1128 (V)	mm
Driver IC	HX8279	-
Operation Temperature	-10~60	℃
Storage Temperature	-20~70	℃

1.2 Touch Panel Information

Item	Specification
Touch Structure	G+G
Bonding Type with LCM	OCA Optical Bonding
Driver IC	GT928
Interface	I²C
Touch Count Max	10 Points
Surface treatment	-
Surface hardness	6H
I2C slave address	0x28
Origin of coordinate	Down right Corner

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	VDD_3.3V	-0.3	5.0	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

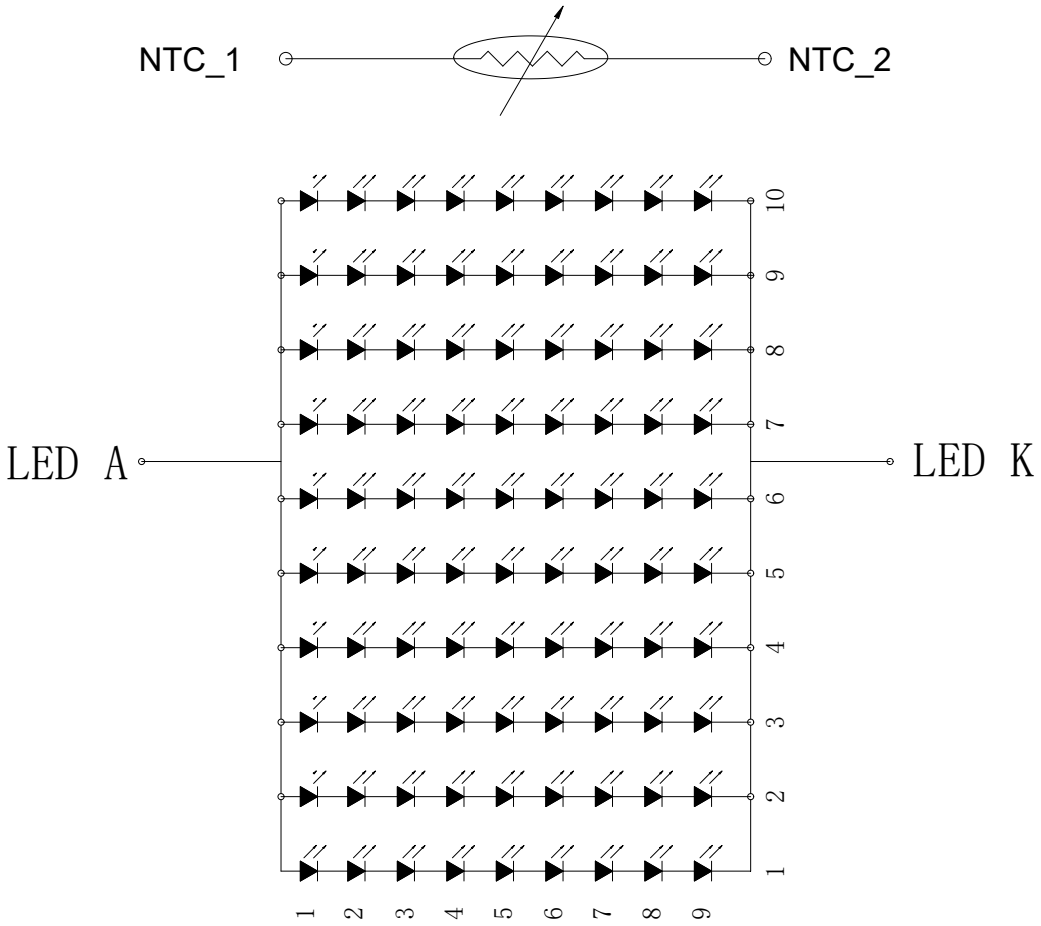
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VDD_3.3V	3.0	3.3	3.6	V	
Analog supply current	$I_{VDD\_3.3V}$	-	TBD	-	mA	VDD_3.3V=3.3 V
Logic input voltage	VIH	0.7*VDD_3.3 V	-	VDD_3.3V	V	
	VIL	GND	-	0.3*VDD_3.3 V	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	390	-	mA	
Driving Voltage	V_F	24.3	-	30.6	V	
Power consumption	W_{BL}	9.477	-	11.934	W	
LED Life-Time	N/A	-	50,000	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



3.3 Touch Panel

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply voltage	VDD_CTP_3.3V	-	3.3	-	V	
Analog supply current	$I_{VDD\_CTP\_3.3V}$	-	TBD	-	mA	VDD_CTP_3.3V=3.3V
Input high-level voltage	VIH	1.35	1.8	2.1	V	
Input low -level voltage	VIL	GND	-	0.45	V	

4. Interface Pin Assignment

4.1 LCM Pin Assignment

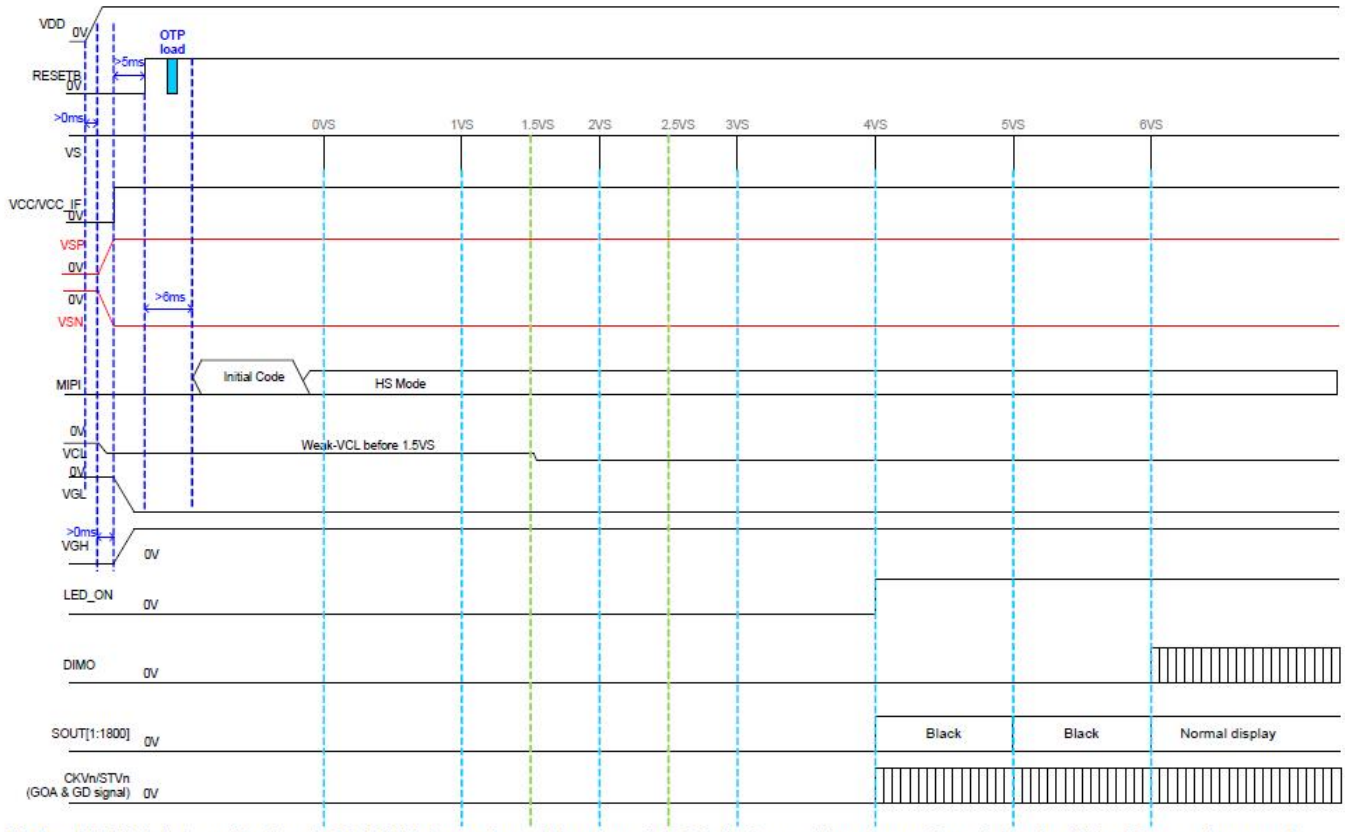
No.	Symbol	Description
1	NC	No connection
2-3	VDD_3.3V	Power supply (3.3V)
4	NC	No connection
5	RESET_1.8V	Global reset pin (1.8V)
6	NC	No connection
7	GND	Ground
8	MIPI_D2N	MIPI Negative data signal(-)
9	MIPI_D2P	MIPI Positive data signal(+)
10	GND	Ground
11	MIPI_D1N	MIPI Negative data signal(-)
12	MIPI_D1P	MIPI Positive data signal(+)
13	GND	Ground
14	MIPI_CKN	MIPI Positive clock signal(+)
15	MIPI_CKP	MIPI Negative clock signal(-)
16	GND	Ground
17	MIPI_D0N	MIPI Negative data signal(-)
18	MIPI_D0P	MIPI Positive data signal(+)
19	GND	Ground
20	MIPI_D3N	MIPI Negative data signal(-)
21	MIPI_D3P	MIPI Positive data signal(+)
22	GND	Ground
23-24	NC	No connection
25	GND	Ground
26	NC	No connection
27	NTC1(NC)	No connection
28	NTC2(NC)	No connection
29	NC	No connection
30	GND	Ground
31-32	VLED-	Power for LED backlight (Cathode)
33	VDD_CTP_3.3V	Power supply for CTP (3.3V)
34	GND_CTP	Ground
35	SDA_CTP_1.8V	I2C data input and output for CTP (1.8V)
36	SCL_CTP_1.8V	I2C clock input for CTP (1.8V)
37	INT_CTP_1.8V	Interrupt signal for CTP (1.8V)
38	RST_CTP_1.8V	Reset Pin for CTP (1.8V)
39-40	VLED+	Power for LED backlight (Anode)

5. Interface Characteristics

5.1 Power on/off sequence

5.1.1 Power on sequence PWRMD=1→Max. Power on time=6.0VS

After reset state or exit STB mode, the power on sequence will start. One SCHOTTKY diode is necessary between VGL and GND when VDD and VSP start at the same time.



Note: (1) Finish to write the GOA MUX (page1 registers) and GOA timing setting (page3 registers) within 50ms after reset pulls to high

Figure 5.7: Power on sequence with PWRMD=1 and repair OP disable

5.1.2 Power off sequence PWRMD=1→Max. Power off time=4.5VS

When enter STB mode, the STBYB signal will be set to low then the power off sequence will start.

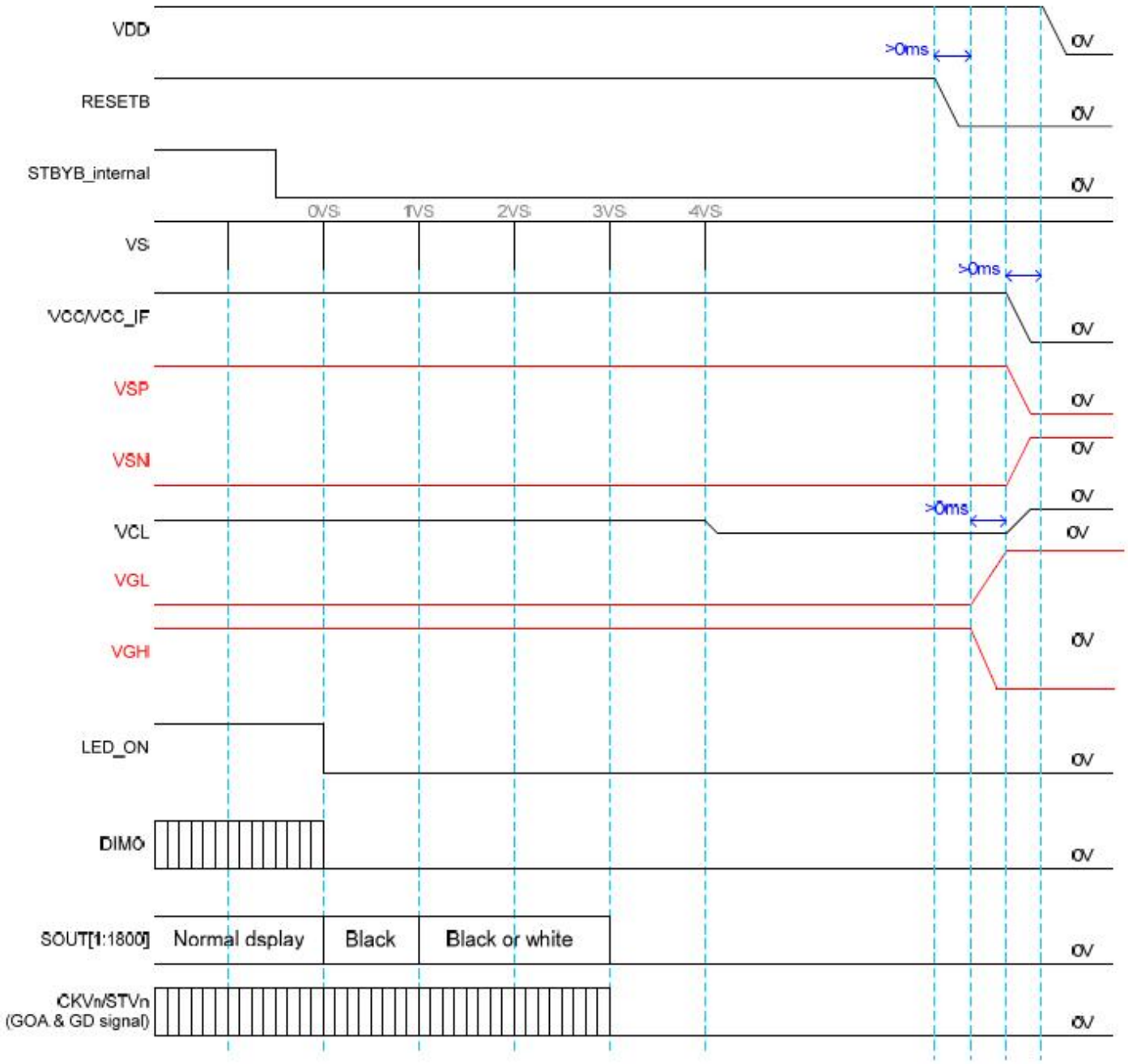


Figure 5.8: Power off sequence with PWRMD=1

5.2 AC Characteristics

5.2.1 MIPI AC characteristics

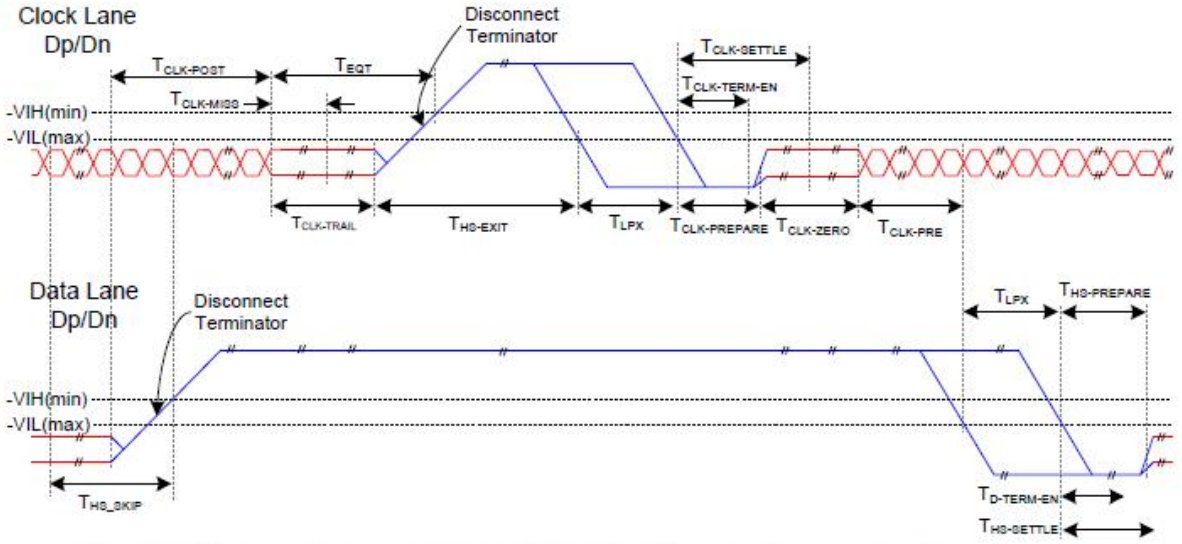


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

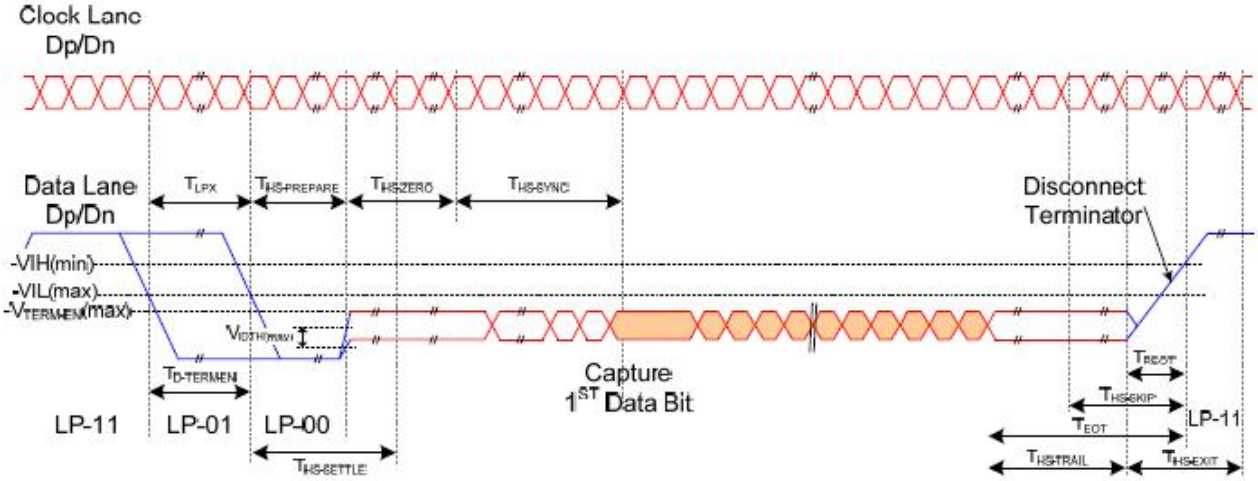


Figure 13.2: Timing of high-speed data transmission in bursts

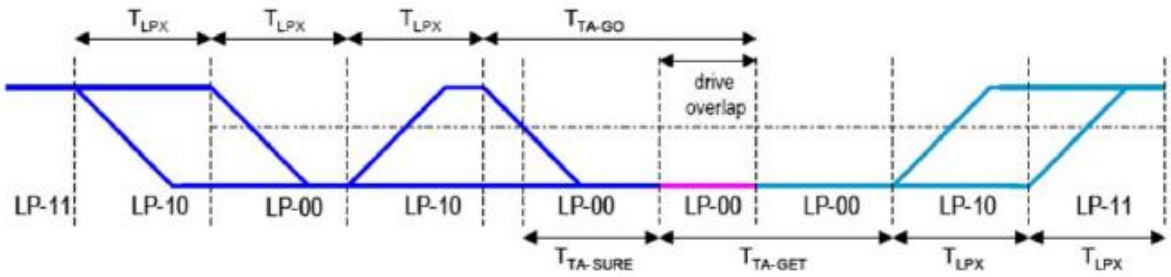


Figure 13.3: Turnaround Procedure

MIPI AC Characteristics

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI (For DCS)	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$(1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	5*T_{LPX}			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	4*T_{LPX}			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	2*T_{LPX}	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

5.2.2 MIPI data-clock timing specification

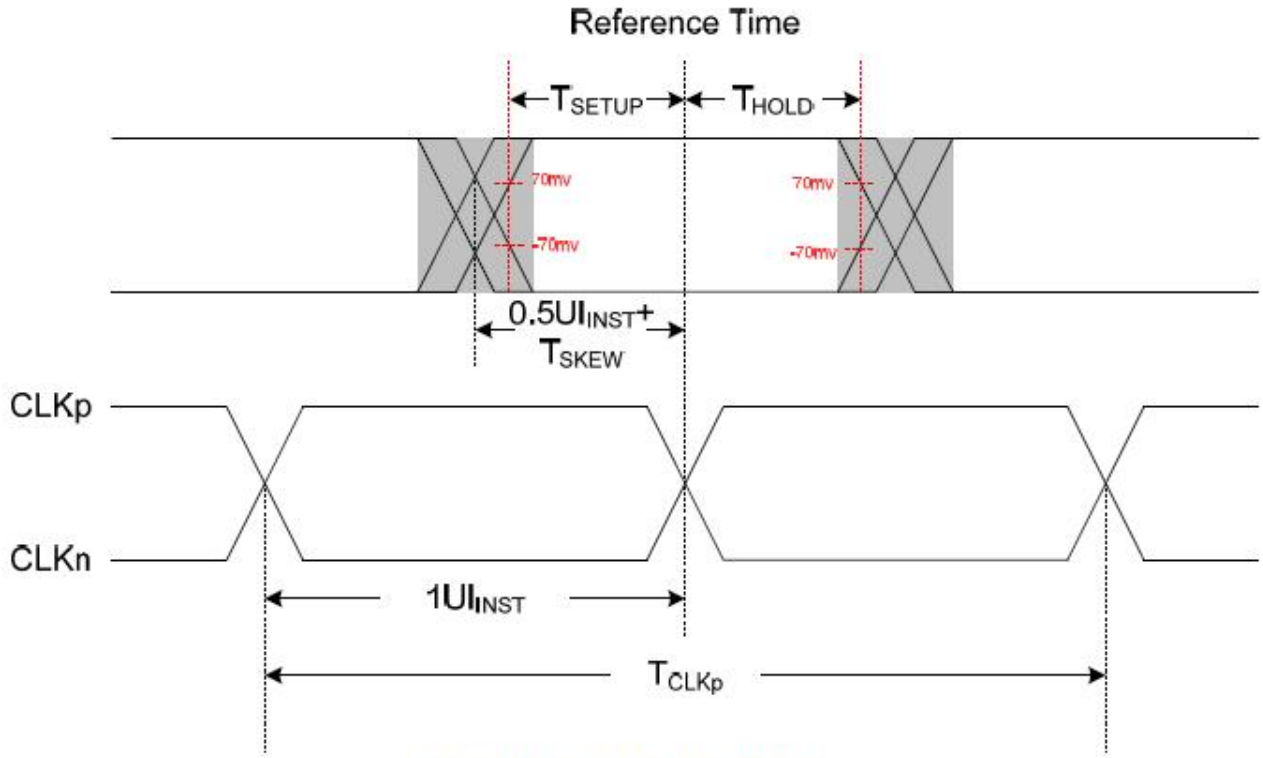
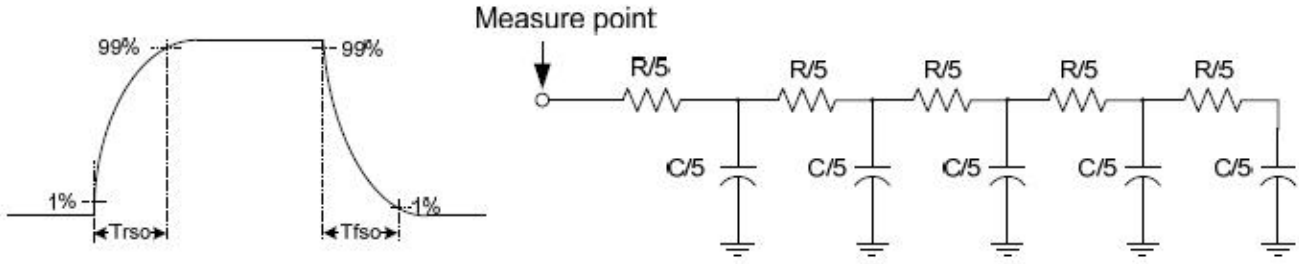


Figure 13.4: Data to clock timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous	UI_{INST}	1.0	-	12.5(1)	ns
Data to clock setup time	T_{SETUP}	0.15	-	-	UI_{INST}
Data to clock hold time	T_{HOLD}	0.15	-	-	UI_{INST}

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

5.2.3 Source output timing

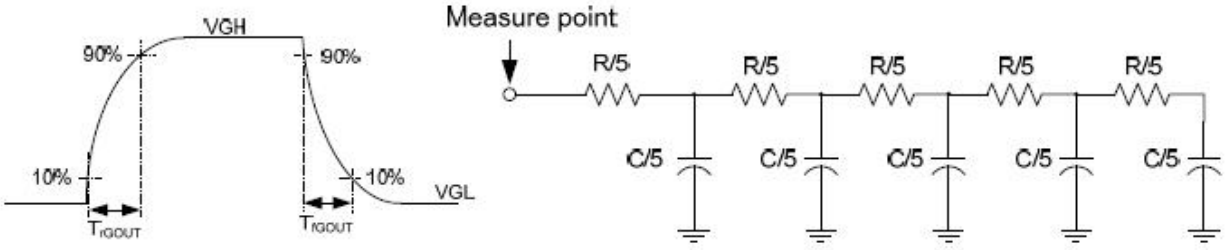


Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Source driver rising time	trSO	Load R=7.94KΩ, Load C = 85.84pF, Voltage: -5V←→5V VSN=-5.1V, VSP=5.1V	-	-	6.0	µs
Source driver falling time	tfSO		-	-	6.0	µs

Note: (1) Himax can support simulation for customer design.

Table 13.1: Source output timing

Panel control signal output 1 **(GOUT1_L~GOUT20_L, GOUT1_R~GOUT20_R)**

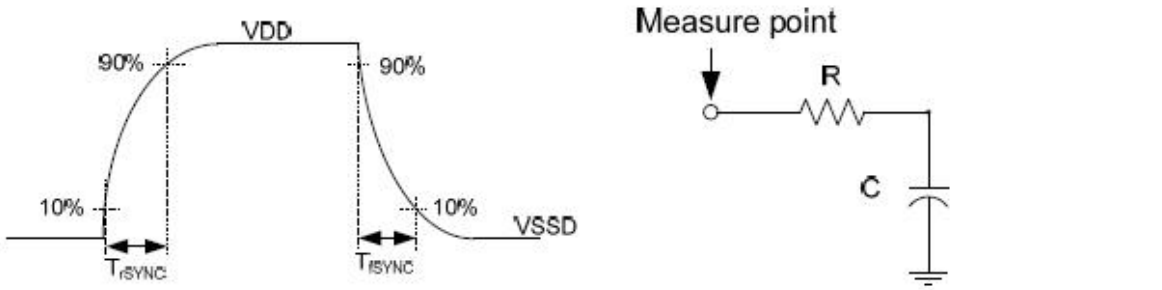


Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Panel control signal rising time	T_{rGOUT}	LOAD R=1780Ω LOAD C=1273pF VGH=+16V, VGL=-16.0V	-	-	5	µs
Panel control signal falling time	T_{fGOUT}		-	-	5	µs

Note: (1) Himax can support simulation for customer design.

Table 13.2: GOA output timing

Panel control signal output 2 **(SYNC1_L~ SYNC8_L, SYNC1_R~ SYNC8_R)**



Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Panel synchronization signal rising time	T_{rSYNC}	LOAD R = 1KΩ	-	-	60	ns
Panel synchronization signal falling time	T_{fSYNC}	LOAD C = 40pF	-	-	60	ns

Note: (1) Himax can support simulation for customer design.

Table 13.3: Synchronization signals output timing

5.2.4 Serial interface characteristics

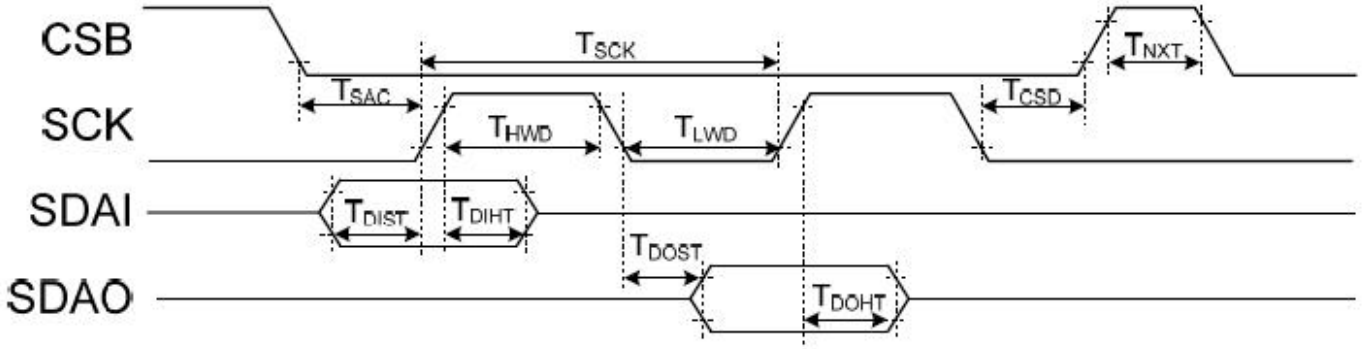


Figure 13.5: Serial interface characteristics

(VSS=0V, VDD=1.7~2.0V, TOPR =-20 to 85℃)

Parameter	Symbol	Conditions	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
CSB assertion to first clock edge	T_{SAC}	-	120	-	-	ns
CSB reassertion from last clock edge	T_{CSD}	-	120	-	-	ns
CSB next control enable	T_E	-	200	-	-	ns
SCK period time	T_{SCK}	-	200	-	-	ns
SCK high period time	T_{HWD}	-	100	-	-	ns
SCK low period time	T_{LWD}	-	100	-	-	ns
SDAI input data setup time	T_{DIST}	-	50	-	-	ns
SDAI input data hold time	T_{DIHT}	-	50	-	-	ns
SDAO output data setup time	T_{DOST}	-	60	-	100	ns
SDAO output data hold time	T_{DOHT}	-	60	-	100	ns

Table 13.4: AC characteristic of SPI interface

5.2.5 Timing requirements for RESETB

The closed interval of low can be shown as the following.

(VDD=1.7V~2.0V, VSS=0V, TOPR =-20℃~+85℃)

Parameter	Symbol	Conditions	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Reset low pulse width	Trst	-	20	-	-	μs

Table 13.5: Reset timing

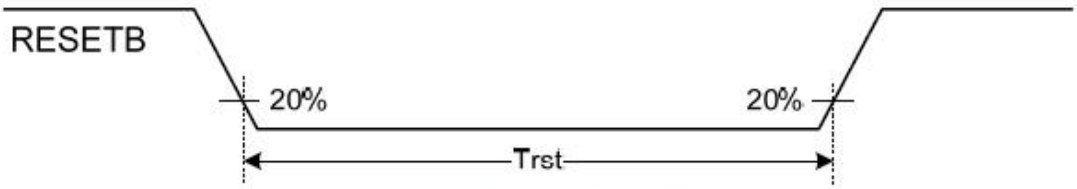


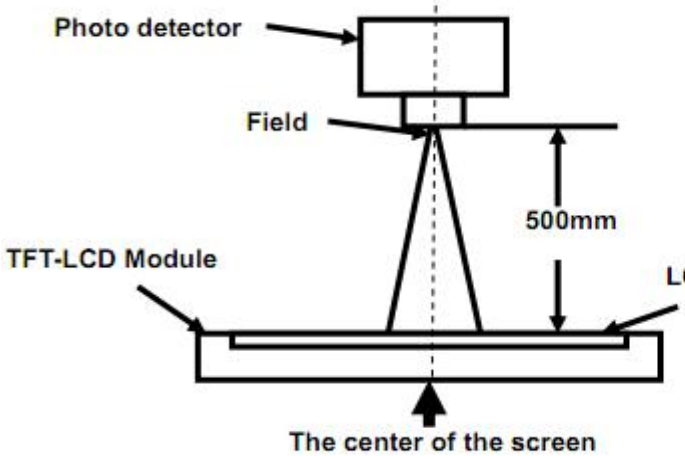
Figure 13.6: Reset timing

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	80	85	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	80	85	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	80	85	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	80	85	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	12	-	msec	Note4
	T_{OFF}		-	12	-	msec	Note4
Contrast Ratio	CR		800	1000	-	-	Note1 Note3
Color Chromaticity	W_X		TBD	TBD	TBD	-	Note1 Note5
	W_Y		TBD	TBD	TBD	-	Note1 Note5
Luminance	L		1300	1500	-	cd/m²	Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		-	65	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Fig 1

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

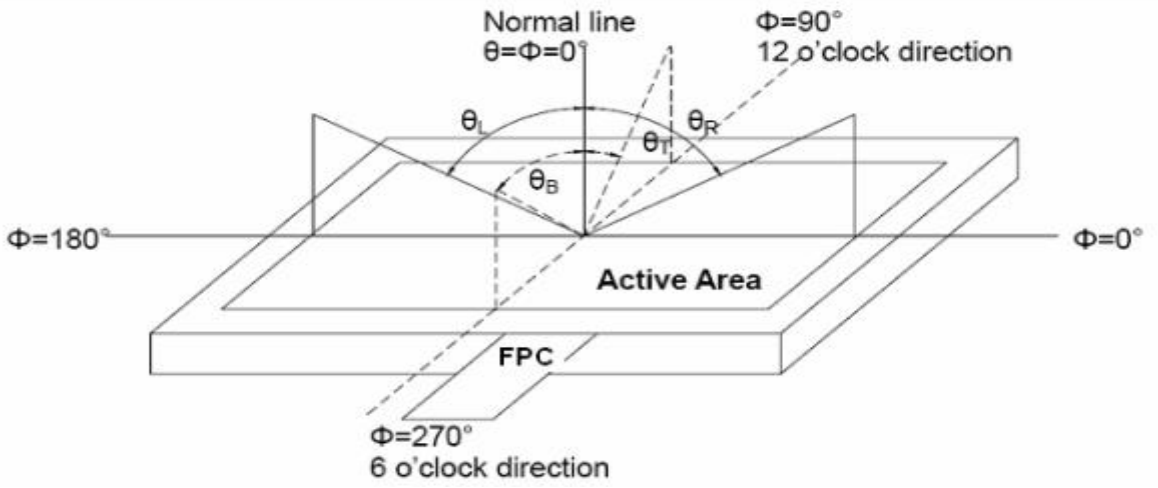


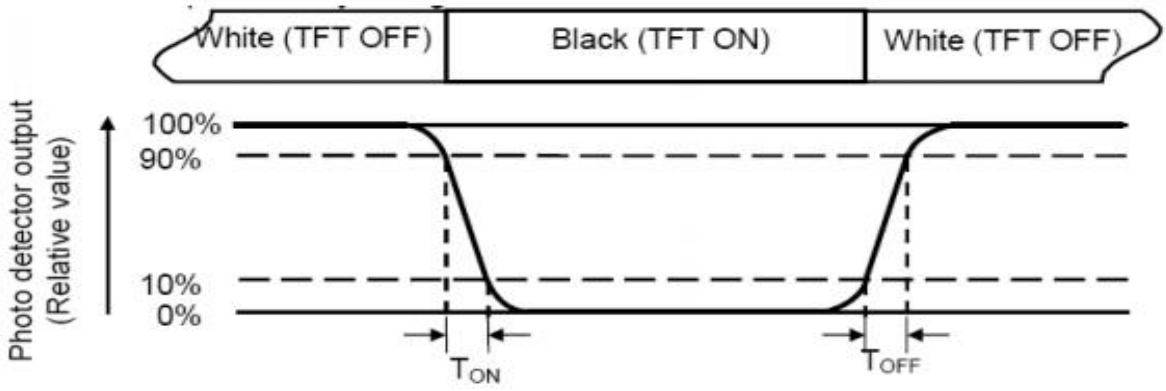
Fig 2 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.3-a/b

Note 7:Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

For more information see FIG.3-a/b

Note 8:Size : S≤5”(see Figure a) A : 5 mm B : 5 mm. H,V : Active area

Light spot size ⌀ =5mm(BM-5) or ⌀=7.7mm (BM-7)50cm distance or test spot position : see Figure a.

measurement instrument : TOPCON’s luminance meter SR-3A or BM-7 or compatible (see Figure 1).

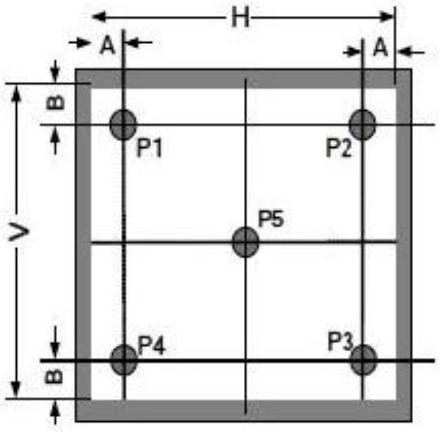


Fig. 3-a Definition of points

5”＜S≤12.3”(see Figure b) . H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens. test spot position : see Figure b.
measurement instrument : TOPCON’s luminance meter SR-3A or BM-7 or compatible (see Figure 1).

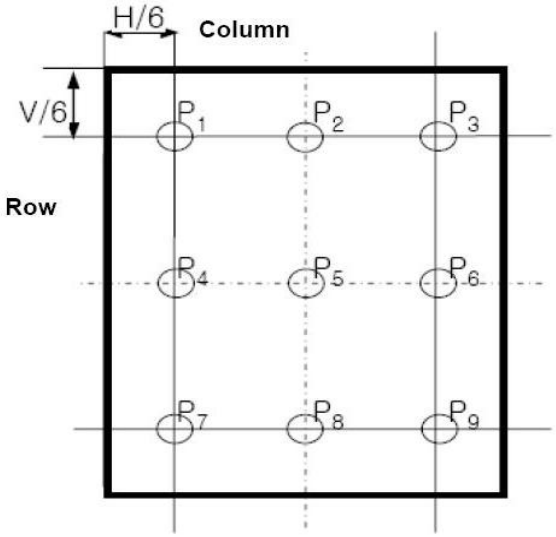


Fig. 3-b Definition of points

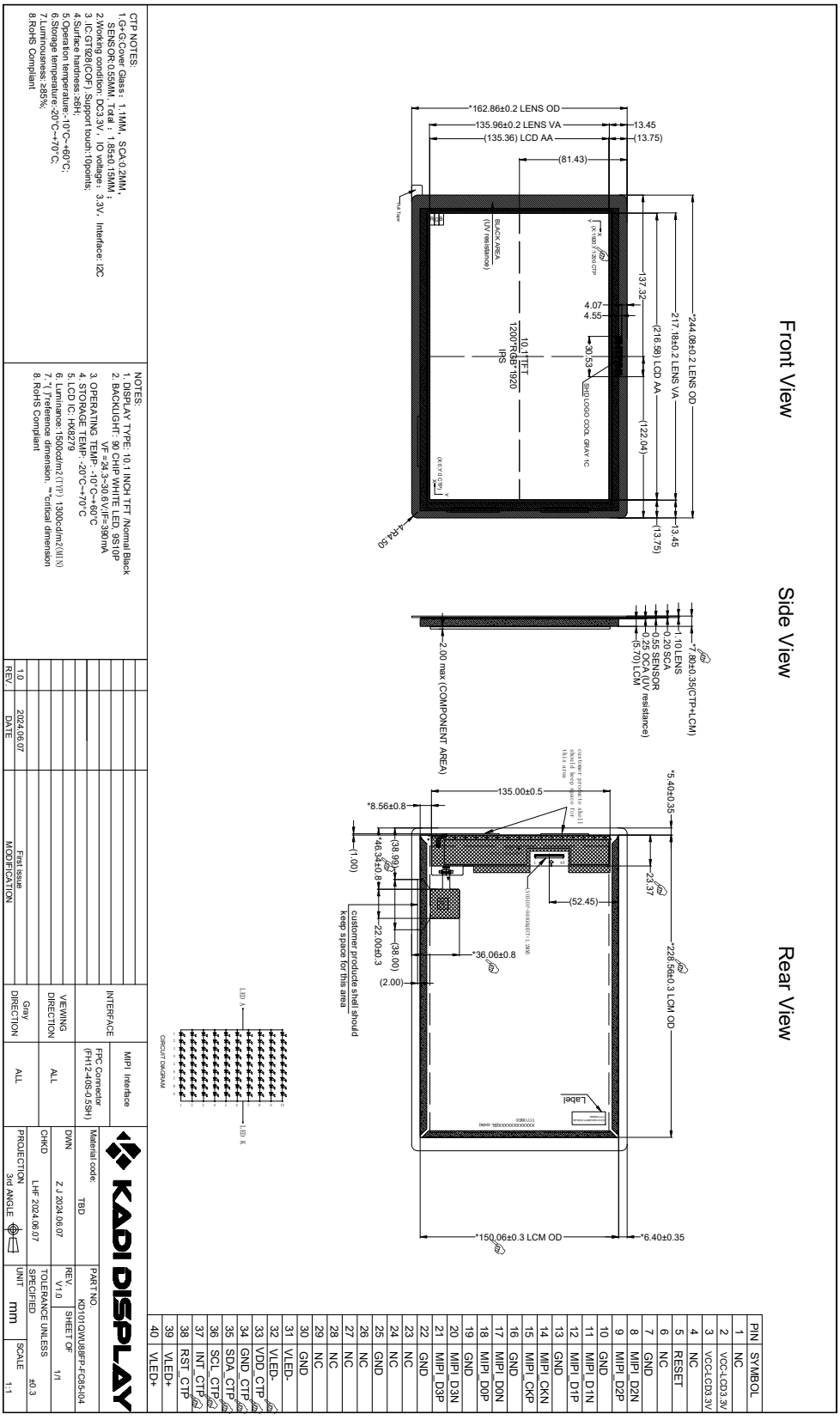
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +70℃	96hrs
Low Temperature Storage	Ta= -20℃	96hrs
High Temperature Operation	Ta= +60℃	96hrs
Low Temperature Operation	Ta= -10℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-20℃/30 min ~ +70℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing



PIN	SYMBOL
1	NC
2	VCC-LCD3.3V
3	VCC-LCD3.3V
4	NC
5	RESET
6	NC
7	GND
8	MIPI_D2N
9	MIPI_D2P
10	GND
11	MIPI_D1N
12	MIPI_D1P
13	GND
14	MIPI_CKN
15	MIPI_CKP
16	GND
17	MIPI_D0N
18	MIPI_D0P
19	GND
20	MIPI_D3N
21	MIPI_D3P
22	GND
23	NC
24	NC
25	GND
26	NC
27	NC
28	NC
29	NC
30	GND
31	VLED-
32	VLED-
33	VDD_CTP
34	GND_CTP
35	SDA_CTP
36	SCL_CTP
37	INT_CTP
38	RST_CTP
39	VLED+
40	VLED+

CTP NOTES:
1.G+G,Cover Glass : 1.1MM, SCA:0.2MM, SENSOR:0.55MM ; Total : 1.85±0.15MM ;
2.Working condition: DC:3.3V ; IO voltage : 3.3V, Interface: I2C
3.10 Finger touch, support touch:10points;
4.Surface hardness: ≥6H;
5.Operation temperature:-10℃~+60℃;
6.Storage temperature:-20℃~+70℃;
7.Luminousness: ≥85%;
8.RoHS Compliant

NOTES:
1. DISPLAY TYPE: 10.1 INCH TFT /Normal Black
2. BACKLIGHT: 90 CHIP WHITE LED, 9S10P
VF =24.3~30.6V,IF=390mA
3. OPERATING TEMP: -10°C~+60°C
4. STORAGE TEMP: -20°C~+70°C
5. LCD IC: HX8279
6. Luminance:1500cd/m2(TYP) 1300cd/m2(MIN)
7. '( )'reference dimension, '*'critical dimension
8. RoHS Compliant

REV.	DATE	MODIFICATION
1.0	2024.06.07	First issue

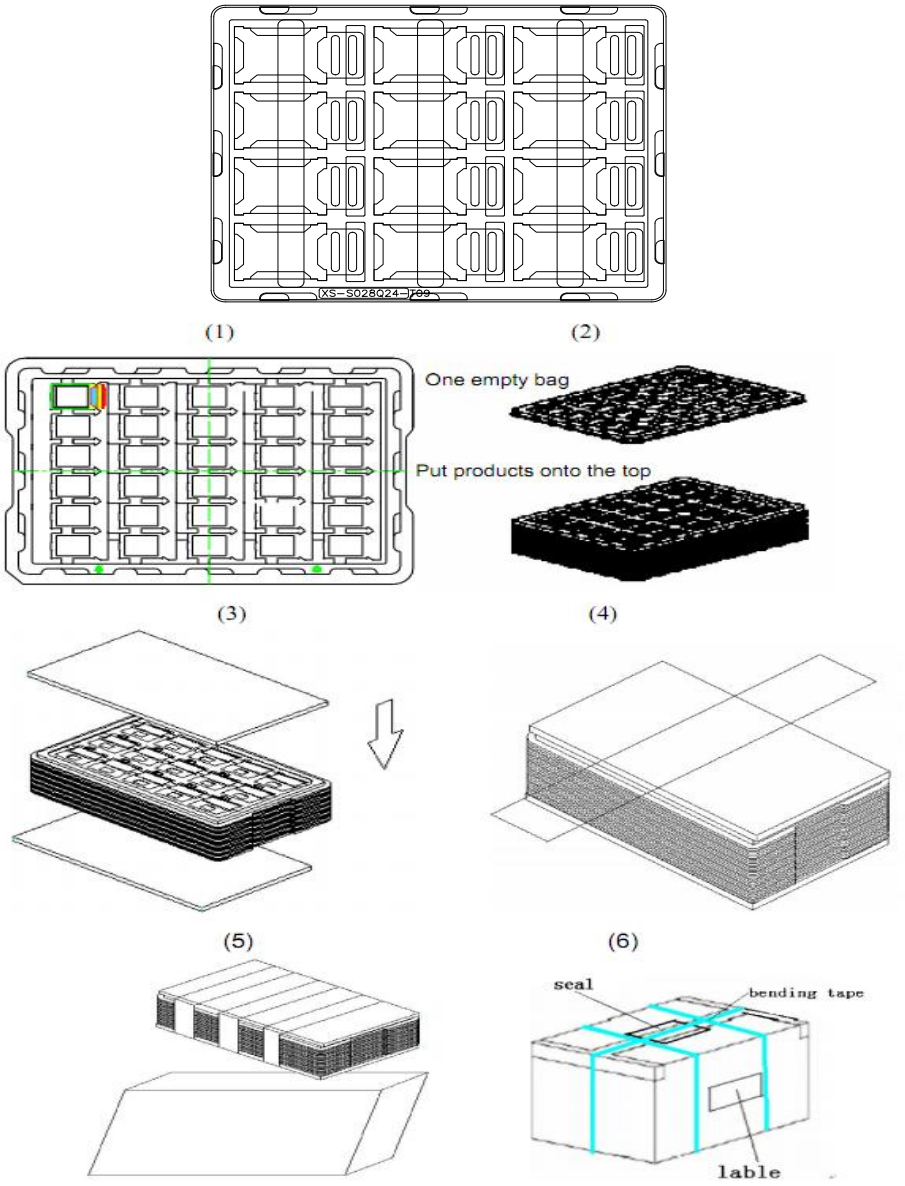
INTERFACE	MIPI Interface	
VIEWING DIRECTION	ALL	FPC Connector (FH12-40S-0.5SH)
Gray DIRECTION	ALL	

KADI DISPLAY

PROJECTION	3rd ANGLE	Material code: TBD
CHKD	Z J 2024.06.07	PART NO. KD1010QWU88FP-FC85-I04
DWN	LHF 2024.06.07	REV. V1.0 SHEET OF 1/1
UNIT	mm	TOLERANCE UNLESS SPECIFIED ±0.3
SCALE	1:1	

9. Packing

Packing Method



Steps:

1. Put module into tray cavity
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above
4. Fix the cardboard to the tray stack with adhesive tape
5. Put the tray stack into carton
6. Carton sealing with adhesive tape

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.